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PROGRAMMABLE PARALLEL FBD SIGMA DELTA ADC RECONSTRUCTION STAGE DESIGN FOR SOFTWARE DEFINED RADIO RECEIVER

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Abstract: Today's bottleneck of signal processing in multistandard software defined radio (SDR) receiver is the analog-to-digital converter (ADC). Therefore, the authors present in this paper the design and simulation results of a programmable parallel frequency band decomposition (FBD) architecture for ADC. The designed parallel architecture is composed of six parallel branches based on discrete-time (DT) 4th order sigma delta modulators using single-bit quantizers. Each branch processes a sub-bandwidth of the received signal. Only needed branches are selected according to the chosen standard. The parallel sigma delta modulators' outputs are handled by a demodulation-based digital reconstruction stage in order to provide the FBD sigma delta-based ADC output signal. The digital reconstruction stage differs from one communication standard to another. In this paper, its design is discussed for the UMTS use case. The objective is to propose a digital reconstruction design with optimized complexity. In fact, the authors propose a comparative study between some configurations of demodulation, decimation and filtering processes. Technical choices and simulation results are discussed. For UMTS use case, the proposed FBD sigma delta-based ADC architecture ensures a computed signal-to-noise ratio (SNR) over 74 dB.

Keywords: Sigma delta modulators, frequency band decomposition architecture, software defined radio receiver, wireless communication standards, digital reconstruction.

1. INTRODUCTION

Software defined radio (SDR) technology is a state-of-the-art technology solution proposed by scientists to achieve a feasible multistandard receiver [1]. It permits at many coexistent wireless systems to be implemented using common radio platform architecture [1-2]. SDR concept consists in implementing as much as possible of the radio features in software in order to minimize analog circuitry. Therefore, software brings flexibility and adaptability to multistandard receiver while increasing design constraints on the analog-to-digital converter (ADC). In fact, the ADC has to digitize signals from narrowband to wideband with different required dynamic ranges [3-5]. Nonetheless, in the literature, there is no such a fully-integrated ADC that fulfills SDR constraints [6-7]. To overcome this problem, the authors propose the use of parallel architectures based on ΣΔ modulators that ensure high dynamic range while extending signal conversion bandwidth [8].

In fact, ΣΔ modulators present notable interest thanks to their high accuracy. They can reach high resolutions over 16 bits [6]. However, their main drawback is the limited conversion bandwidth due to the noise shaping that requires oversampling [9]. Parallel architectures are therefore used to avoid this limitation. Parallel architectures are time-interleaved sigma delta (TIΣΔ) [10], parallel Hadamard sigma delta (ΠΣΔ) [11] and frequency band decomposition (FBD) [12-13]. Parallelism using FBD permits extending ΣΔ modulators to wideband applications without the drawbacks of TIΣΔ and ΠΣΔ architectures [8]. In fact, FBD architecture is not sensitive to gain and offset mismatches [14-15]. FBD is a natural way to extend bandwidth since each ΣΔ modulator of the parallel architecture converts a part of the input signal bandwidth [12-13,

16]. The parallel modulators' outputs are combined using a digital reconstruction stage to form the final output [16]. Accordingly, the authors take advantage of FBD architecture to design a parallel ΣΔ-based ADC architecture intended for an SDR receiver that processes E-GSM, UMTS and IEEE802.11a communication signals. The proposed FBD architecture is composed of six programmable branches based on discrete-time (DT) 4th order ΣΔ modulators [17]. The modulators use single-bit quantization to overcome non-linearity errors introduced by multi-bit quantizers [13].

In the literature, authors propose in [12-13, 16] an FBD ΣΔ-based ADC architecture that is a generic parallel architecture composed of ten 3rd order continuous-time (CT)-ΣΔ modulators. This architecture operates at 800 MHz-sampling frequency with a total conversion bandwidth of 80 MHz that is uniformly shared between the parallel branches. Each branch processes 8 MHz of signal bandwidth and the architecture realizes a resolution of 13.3 bits. However, in this paper, the novelty is the design of the reconstruction stage of an FBD ΣΔ-based ADC architecture for E-GSM, UMTS and IEEE802.11a communication standards. Indeed, the parallel branches are programmable with different sub-bandwidths, where only some branches are active according to the selected standard. The sampling frequency also changes with the chosen standard. The selected branches for a given standard can be reused for the signal digitization of another standard according to the specified sampling frequency and branches' bandwidths configuration. Besides, ΣΔ modulators of the proposed FBD architecture are implemented in discrete-time (DT) instead of continuous-time (CT) as in [12] in order to avoid analog errors.

This paper includes three sections. In section 2, the authors present the system level specifications for the E-GSM, UMTS and IEEE802.11a SDR receiver. Besides, the design results of a programmable FBD ΣΔ-based ADC architecture for the multistandard SDR receiver are given. In section 3, the digital reconstruction stage design of the FBD ΣΔ-based ADC is discussed. The authors start from conventional demodulation-based digital reconstruction architecture. Then, modifications are proposed regarding complexity studies. Configurations of two-stage decimation are compared in order to choose the best configuration that provides the lowest complexity. Afterwards, the obtained FBD ΣΔ-based ADC with the optimized digital reconstruction stage is implemented on MATLAB/SIMULINK environment and section 4 deals with simulation results. Finally, section 5 draws some conclusions and future works.

2. FBD ΣΔ-BASED ADC ARCHITECTURE FOR SDR RECEIVER

As today's bottleneck of signal processing in multistandard SDR receiver is the ADC, the authors need to study a novel ADC architecture. Therefore, in this section, SDR receiver system level specifications are presented in the first sub-section. Then, the second sub-section presents FBD ΣΔ-based ADC architecture design results.

2.1. SYSTEM LEVEL SPECIFICATIONS

In the first hand, the proposed SDR receiver processes E-GSM, UMTS and IEEE802.11a signals [17]. According to these communication standards, design specifications for the multistandard receiver front-end are depicted. In fact, Table 1 summarizes the channel bandwidth and spacing (Ch_{BW} and Ch_{sp}, respectively), the reference sensitivity (S_{ref}), the signal-to-noise ratio at the receiver input and at the receiver output (SNR_{in} and SNR_{out}, respectively), the analog gain relative to a 13 dBm ADC full scale input (G_{ana}), the receiver dynamic range (DR_{in}) and the ADC dynamic range (DR_{ADC}) from which the ADC resolution (Res_{ADC}) is deduced.

Table 1. design specifications for E-GSM/UMTS/IEEE802.11a receiver.

	E-GSM	UMTS	IEEE802.11a (54 Mbits/s)
Ch_{BW} (MHz)	0.2	3.84	16.6
Ch_{sp} (MHz)	0.2	5	20
S_{ref} (dBm)	-102	-117	-65
SNR_{in} (dB)	18.8	-9	36.6
SNR_{out} (dB)	9	-18.2	26.6
G_{ana} (dB)	28	38	43
DR_{in} (dB)	87	92	35
DR_{ADC} (dB)	96	73.8	61.8
Res_{ADC} (bits)	16	12	10

In the second hand, a hybrid homodyne/low-IF architecture is presented in [18] for the SDR receiver front-end. The received signals, modulated around the f_{RF} frequency, are first filtered by an RF filter. Second, they are amplified using a low-noise amplifier (LNA). Third, UMTS and IEEE802.11a signals are down-converted by the mixer, which is controlled by the local oscillator (LO), to baseband. However, E-GSM signals are down-converted to a low intermediate frequency which is equal to 100 kHz in order to avoid the flicker noise disturbance [18]. Consequently, the E-GSM channel bandwidth is considered equal to 200 kHz as mentioned in Table 1.

Otherwise, the mixed baseband stage architecture using an FBD-based ADC is presented in Fig. 1. The

mixer is followed by a non-programmable 6th order Butterworth anti-aliasing filter (AAF) that passes all signals in the IEEE802.11a bandwidth and attenuates blockers around sampling frequency. In this case, there is no need to use an automatic gain control (AGC) block before the ADC [18].Then, the ADC is designed as a parallel architecture based on FBD architecture and using M DT-ΣΔ modulators. It needs to be followed by a digital reconstruction stage that reconstruct the final output signal from the parallel ΣΔ modulators' output signals while operating decimation and channel selection. The design results of the FBD-based ADC architecture are summarized in the next sub-section.

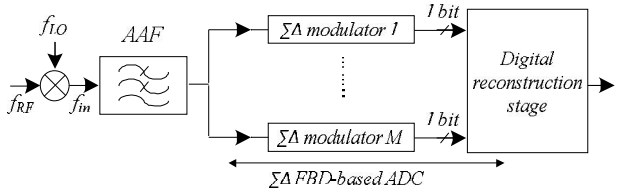

Fig. 1 – ΣΔ FBD-based mixed baseband architecture.

2.2. FBD ΣΔ-BASED ADC ARCHITECTURE DESIGN RESULTS

Starting from system level specifications according to the communication standards handled by the SDR receiver, an FBD ΣΔ-based ADC architecture design is presented. Design specifications for the multistandard receiver impose high constraints on the ADC stage. In fact, a high dynamic range equal to 96 dB is required for narrowband E-GSM signals with 200 kHz channel bandwidth in contrast to a weaker required dynamic range of 61.8 dB for wideband IEEE802.11a signals whose channel bandwidth is equal to 16.6 MHz as shown in Table 1. Therefore, the design of the parallel ADC realizes a trade-off between increasing the sampling frequency while choosing discrete-time ΣΔ modulators but also increasing the number of parallel branches regarding a low-complexity aim, and increasing ΣΔ modulators orders while ensuring their stability [19]. Thus, an FBD design architecture composed of six programmable parallel branches is proposed as presented in Fig. 2 [17]. The first branch uses a 4th order discrete-time (DT) low-pass (LP) ΣΔ modulator. The remaining five other branches are based on 4th order DT band-pass (BP) ΣΔ modulators. The ΣΔ modulator order is defined as the number of integrators or resonators, *p*, for LP or BP ΣΔ modulators, respectively. Since the designed FBD architecture is composed of both LP and BP ΣΔ modulators, the authors designate *p* as ΣΔ modulator order [17].

The proposed design is programmable since according to the selected communication standard, only some branches are active. Sampling frequency choice also modifies operating ΣΔ modulators' sub-bandwidths of the selected branches. This is defined as in the branch frequency division plan presented by Fig. 3 [17].

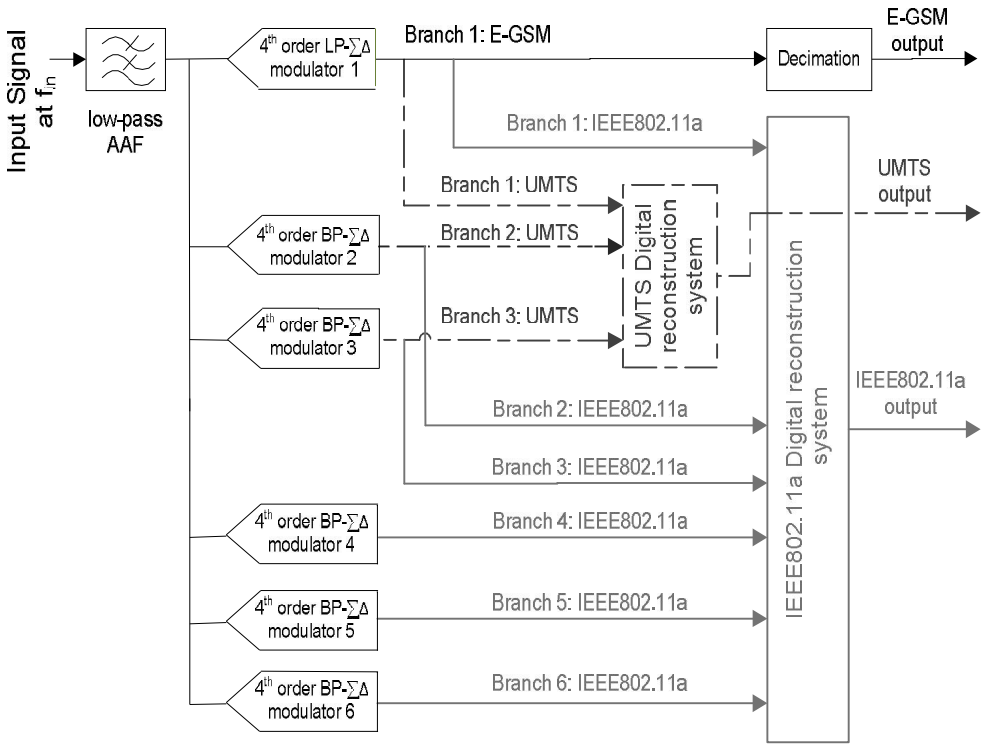

Fig. 2 – Designed FBD ΣΔ-based ADC architecture.

Indeed, the branches that digitize a given standard's signals can be reused to digitize another standard's signals. This leads to a final flexible architecture. For this architecture, sampling frequencies are lower than 100 MHz to permit synthesizing the ΣΔ modulators of the designed FBD architecture in discrete-time domain and thus avoiding analog errors. In fact, the discrete-time technology limits sampling frequencies for the ΣΔ modulators [6].

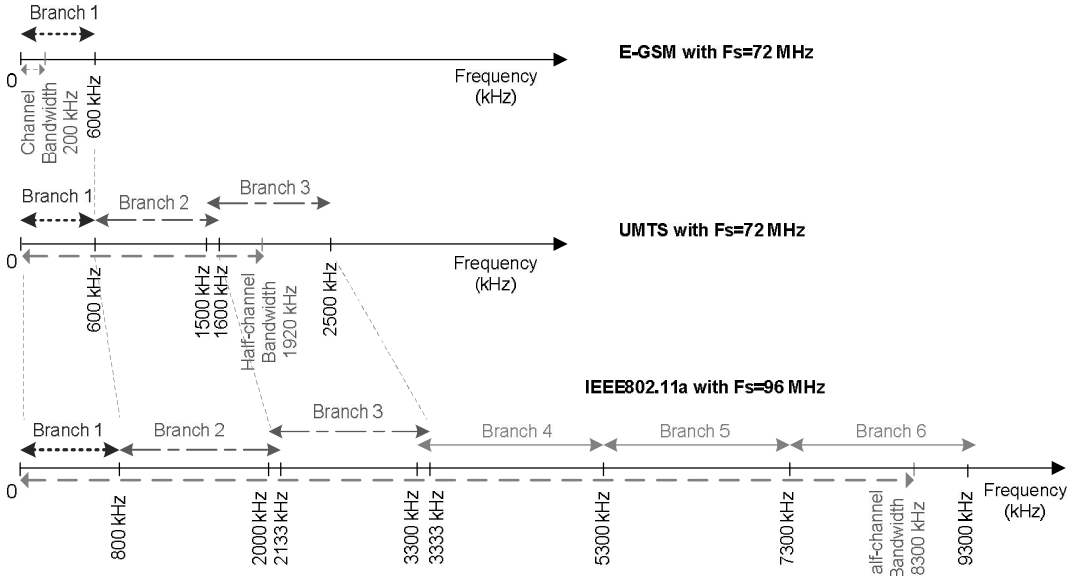

Fig. 3 – Branch frequency division plan.

A digital reconstruction stage is required to combine the parallel ΣΔ modulators outputs of the FBD architecture in order to recover the final output signal. The design of this stage is discussed in the next section.

3. DIGITAL RECONSTRUCTION STAGE DESIGN

In the literature, for digital reconstruction process, there are two main solutions which are the direct reconstruction and the demodulation-based digital reconstruction [12]. The first solution is based on BP filters placed at the parallel ΣΔ modulators' outputs. These filters permit selecting useful signals in selected sub-bandwidths. Then, selected parallel signals are summed using an adder that is followed by a decimation operation. The reconstructed final output is therefore obtained. The main drawback of this direct reconstruction is that the BP filters present high complexity since they operate at the oversampling frequency of the ΣΔ modulators [12]. The second approach for digital reconstruction based on demodulation offer a solution to this problem.

In fact, the BP ΣΔ modulators' output signals are firstly down-converted to baseband thanks to a complex demodulation operation. For the first branch, since the ΣΔ modulator is LP, there is no need to perform demodulation. Secondly, after demodulation of BP modulators' output signals, a decimation process is applied to the baseband signals before their selection by LP filters. The LP filters in the demodulation-based reconstruction approach present lower complexity compared with BP filters of the direct reconstruction approach since they operate at Nyquist sampling frequency. Consequently, in this section, the authors take advantage of the demodulation-based digital reconstruction approach to propose a design for the digital reconstruction stage intended for the proposed FBD ΣΔ-based ADC architecture. The UMTS standard is chosen as a use case study. First sub-section discusses the demodulation position after the ΣΔ modulators. However, in the second sub-section, the authors compare the configurations of two-stage decimation in order to decide on the best configuration that provides the lowest complexity.

3.1. DEMODULATION POSITION STUDY

In conventional demodulation-based digital reconstruction architecture, the BP ΣΔ modulators' output signals are first frequency down-converted to baseband using a complex digital demodulation. This operation consists in multiplying modulators' output signals by a complex sequence $m_k[n]$ as given by (1) where f_{c_k} is the k^{th} central frequency of the k^{th} branch sub-bandwidth, T_s is the oversampling period and n is a positive integer [20].

$$m_k[n] = e^{-2i\pi f_{c\_k} n T_s} \quad (1)$$

Second, after demodulation, a decimation process is mandatory for the baseband signals that are at the oversampling frequency, F_s, which is equal to $1/T_s$. The oversampling frequency, F_s, corresponds to the sampling frequency of the DT ΣΔ modulators. The decimation process permits the sampling frequency reduction of oversampled baseband signals to bring them to the Nyquist frequency which is defined as the double of the channel bandwidth, ChBW. The global decimation factor is equal to the global oversampling ratio, *OSR*, defined as the oversampling frequency, Fs, out of the Nyquist frequency. For the UMTS use case, it is chosen equal to 16. Thus, the UMTS signals are digitized at a Nyquist frequency equal to 4.5 MHz. This Nyquist frequency is comprised between the UMTS channel bandwidth, Ch_{BW}, and channel spacing Ch_{sp}, that are presented in Table 1.

Besides, to implement complex digital demodulation on MATLAB/SIMULINK environment or also for hardware implementation in future works, it is required to use in-phase and quadrature (I/Q) demodulation as illustrated by Fig. 4. Demodulation filters are then needed for I and Q signals to filter out the undesired component of the digital mixer output. After that, to reduce the complexity of decimation filters, a two-stage decimation process is operated. Each decimation stage is composed of decimation filter and down-sampling at rates D_1 or D_2. In the first decimation stage, the authors propose to combine demodulation and decimation filters in order to obtain Filter k.1.I and Filter k.1.Q for the k^{th} branch as shown in Fig. 4. In the second decimation stage, the authors propose to combine branch selection and decimation filters in order to obtain Filter k.2.I and Filter k.2.Q for the k^{th} branch as shown in Fig. 4. Indeed, branch selection filter is required to select the branch sub-bandwidth to attenuate out-of-band ΣΔ modulator quantization noise. After second stage demodulation, since the signals at the parallel branches are in baseband, it is mandatory to perform frequency up-conversion using modulation. The signals are therefore up-converted from baseband to around the central frequency of the adequate branch sub-bandwidth at the Nyquist frequency. Then, the signals are added to obtain the k^{th} branch output signal.

To discuss the demodulation position, the authors start with the demodulation filter design. Table 2 summarizes, for example, demodulation filter design parameters as well as its complexity computation in terms of multiplications per second, *MPS*, for the second branch of UMTS use case.

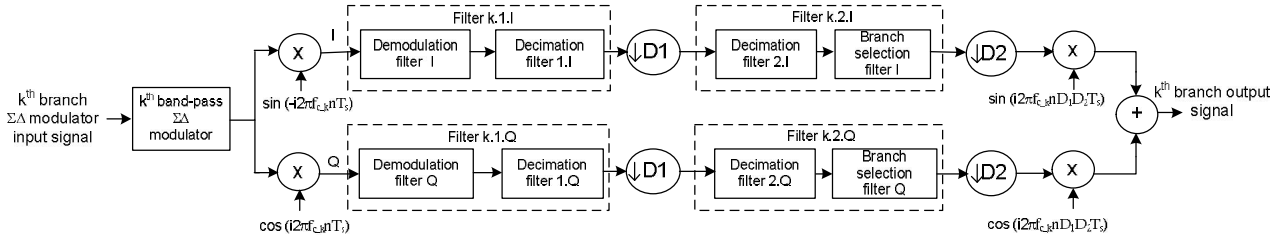

Fig. 4 – k^{th} branch architecture, $2 \le k \le M$, of the demodulation-based digital reconstruction stage where demodulation is after the ΣΔ modulator.

Table 2. UMTS Second branch demodulation filter design: parameters and complexity computation.

	Demodulation filter
Cutoff frequency (MHz)	0.5
In-band maximal attenuation (dB)	0.1
Sampling frequency (MHz)	72
Rejection frequency (MHz)	1.7
Maximum between quantization noise level and blocker level (dBm)	-28
Minimal attenuation (dB)	32.8
Filter order	114
MPS (x 10^6)	8208

These results are identical for both of I and Q demodulation filters. It is shown in Table 2 that the complexity of such a filter is very high. Therefore, the authors opt to modify the digital reconstruction stage architecture and to place the demodulation after the first decimation stage in order to reduce the demodulation filter complexity. This leads to the proposed digital reconstruction architecture of Fig. 5. In the first decimation stage, there are decimation filter k.1 and down-sampling at rate D_1. After demodulation and in the second decimation stage, the authors propose to combine demodulation filter, decimation filter and branch selection filter in order to obtain Filter k.2.I' and Filter k.2.Q' for the k^{th} branch as shown in Fig. 5. In the next sub-section, the authors compare the two-stage decimation configurations when demodulation comes after the first stage decimation.

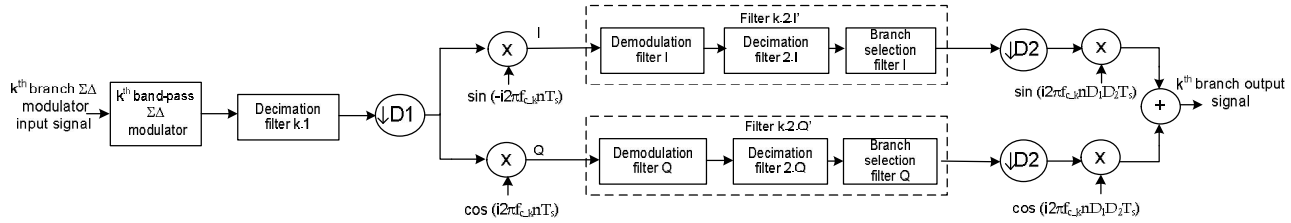

Fig. 5 – k^{th} branch architecture, $2 \leq k \leq M$, of the demodulation-based digital reconstruction stage where demodulation is after the first decimation stage.

3.2. COMPARISON OF TWO-STAGE DECIMATION CONFIGURATIONS

For the 16-global decimation factor, the two-stage decimation configurations D_1xD_2 are 8x2, 4x4 and 2x8. They are studied in order to compare their complexities and choose the less complex one. The results of Filter 2.1, Filter 2.2.I' and Filter 2.2.Q' design parameters, complexity computation and signal-to-noise ratio (*SNR*) for 8x2, 4x4 and 2x8 configurations are presented in Table 3, Table 4 and Table 5, respectively. From theses tables, it is shown that the less complex two-stage decimation configuration is the 8x2 where the first stage ensures decimation by a factor of 8 and the second by 2. In fact, the total *MPS* is equal to 2763 x10^6. However, the 4x4 and 2x8 configurations require much more total *MPS* that are equal to 3780 x10^6 and 11016 x10^6, respectively.

Table 3. Filter 2.1, Filter 2.2.I' and Filter 2.2.Q' design for UMTS Second branch: parameters, complexity computation and SNR for 8x2 decimation configuration.

	Filter 2.1	**Filter 2.2.I' Filter 2.2.Q'**
Cutoff frequency (MHz)	1.6	0.3
In-band maximal attenuation (dB)	0.1	0.1
Sampling frequency (MHz)	72	9
Rejection frequency (MHz)	7.4	0.7
Maximum between quantization noise level and blocker level (dBm)	-18.1 dBm @ 7.4 MHz -12.7 dBm @ 16.4 MHz	-19 dBm @ 0.7 MHz
Minimal attenuation (dB)	42.7 dB @ 7.4 MHz 48.1 dB @ 16.4 MHz	79.8 dB @ 0.7 MHz
Filter order	29	75
MPS (x 10^6)	2088	675
Total *MPS* (x 10^6)	2763	
SNR at the second branch output (dB)	81.08	

Table 4. Filter 2.1, Filter 2.2.I' and Filter 2.2.Q' design for UMTS Second branch: parameters, complexity computation and SNR for 4x4 decimation configuration.

	Filter 2.1	**Filter 2.2.I' Filter 2.2.Q'**
Cutoff frequency (MHz)	1.6	0.3
In-band maximal attenuation (dB)	0.1	0.1
Sampling frequency (MHz)	72	18
Rejection frequency (MHz)	16.4	0.7
Maximum between quantization noise level and blocker level (dBm)	-12.7	-19
Minimal attenuation (dB)	86.1	79.8
Filter order	15	150
MPS (x 10^6)	1080	2700
Total MPS (x 10^6)	3780	
SNR at the second branch output (dB)	76.46	

Table 5. Filter 2.1, Filter 2.2.I' and Filter 2.2.Q' design for UMTS Second branch: parameters, complexity computation and SNR for 2x8 decimation configuration.

	Filter 2.1	Filter 2.2.I' Filter 2.2.Q'
Cutoff frequency (MHz)	1.6	0.3
In-band maximal attenuation (dB)	0.1	0.1
Sampling frequency (MHz)	72	36
Rejection frequency (MHz)	34.4	0.7
Maximum between quantization noise level and blocker level (dBm)	-19	-19
Minimal attenuation (dB)	79.8	79.8
Filter order	3	300
MPS (x 10^6)	216	10800
Total MPS (x 10^6)	11016	
SNR at the second branch output (dB)	74.28	

Moreover, the authors implement the second branch with 8x2, 4x4 and 2x8 decimation configurations on MATLAB/SIMULINK environment. The choice of 8x2 decimation configuration is confirmed thanks to SNR measurements of the second branch output signal. Indeed, SNR are equal to 81.08 dB, 76.46 dB and 74.28 dB for 8x2, 4x4 and 2x8 decimation configurations, respectively. The signals from the parallel branches are finally summed to form the overall final output signal of the FBD ΣΔ-based ADC for the UMTS use case. This architecture is illustrated in Fig. 6.

The next section deals with simulation results of the designed FBD ΣΔ-based ADC architecture using MATLAB/SIMULINK environment.

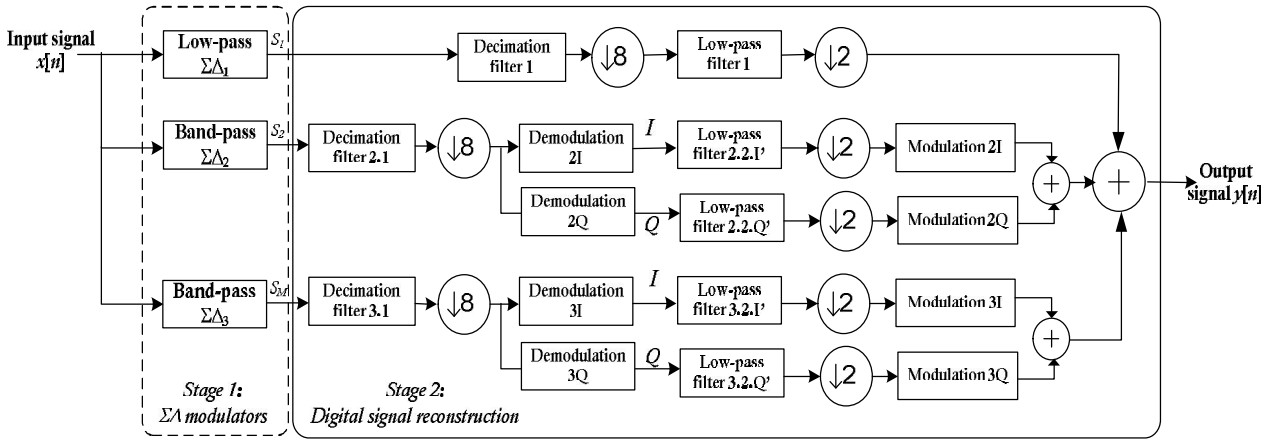

Fig. 6. Proposed demodulation-based digital reconstruction for the FBD ΣΔ-based ADC architecture for the UMTS use case.

4. SIMULATION RESULTS

In this section, the authors start simulation results with SNR measurements for a single-tone input signal at a frequency varying in the UMTS channel bandwidth ($Ch_{BW}/2$). The computed SNR of the FBD ΣΔ-based ADC output signal are presented in Fig. 7. The computed SNR values vary from 68 dB to 73.7 dB. Therefore, it is important to test the designed FBD ΣΔ-based ADC architecture by at least a signal in the operating sub-bandwidth of each branch in parallel to ensure required dynamic range. In practical case, the received modulated signal occupies all the channel bandwidth.

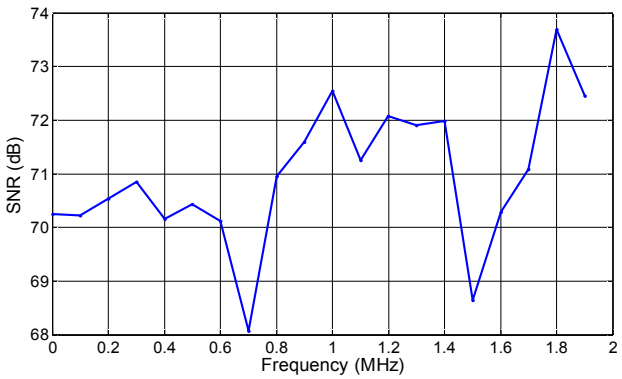

Fig. 7. Computed SNR in UMTS channel bandwidth versus input frequency for a single-tone input signal.

Moreover, simulation results are realized by applying a multi-tone signal which is composed of three sine-wave signals. This signal is applied at the input of the FBD architecture. The sine-wave frequencies values are 300 kHz, 800 kHz and 1900 kHz which belong to the first, second and third sub-bandwidth of the UMTS standard, respectively. The sine-wave normalized amplitudes are set at 0.45. The normalized amplitude is defined as the input amplitude out of the power supply voltage. The recombined final output signal spectrum of the FBD ΣΔ-based ADC which is realized in MATLAB/SIMULINK model is presented in Fig. 8. The SNR of this output signal is computed. The obtained value from the simulation results is equal to 74.63 dB which satisfies the 73.8-dB required dynamic range for UMTS standard. The effective resolution can be deduced from the SNR and reaches 12.1 bits.

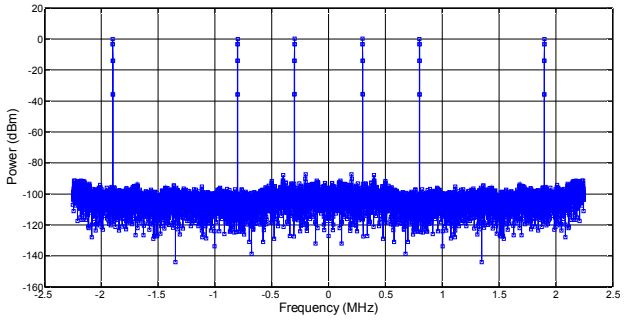

Fig. 8. Spectrum of the FBD ΣΔ-based ADC output signal for UMTS use case.

5. CONCLUSION

In this paper, the demodulation-based digital reconstruction stage design for the frequency band decomposition ΣΔ-based analog-to-digital converter is proposed. This parallel ADC architecture design is intended for multistandard software radio receiver which processes E-GSM, UMTS and IEEE802.11a communication signals. The designed FBD model for UMTS use case, is implemented on MATLAB/SIMULINK environment. The computed signal-to noise ratio of the output signal spectrum is equal to 74.63 dB which is higher than the required UMTS dynamic range. The proposed parallel ADC is programmable and flexible. In future work, the MATLAB/SIMULINK simulated model will be hardware implemented and tested on FPGA.

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