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A QUAD CMOS GATES CHECKING METHOD

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Checking Method.

Abstract: The so-called Fault-Tolerant Systems (FTS) use the structural, temporal, functional, or information redundancy for the achievement of the high reliability. For example, Radiation Hardened by Design (RHBD) Systems are Fault-Tolerant Systems. A Passive FTS, due to a very large structural redundancy (Modular Redundancy), produces faults masking. The Triple Modular Redundancy (TMR) Method has more than 300% redundancy. The Quad Redundancy (QR) Method boasts more than 400% redundancy. The CMOS transistors QR (transistor-level redundancy) is the most effective QR. In this case, no voting element is needed. However, this significantly increases the time delay. In addition, it is necessary to ensure compliance with the Mead-Conway restrictions. QR, in contrast to TMR, raises the problem of checking the redundant structure. The author proposes a QR Checking Method based on a selection of substrates of the CMOS transistors. The power lines of the transistor substrates are separated, which ensures the disconnection of part of the reserve. A simulation confirms the feasibility of the proposed method.

1. INTRODUCTION

Fault-Tolerant Systems (FTS) [1–3] are used in critical areas, for example in space equipment, in nuclear power plants, in medical devices, weapons etc. Passive FTS provide fault-masking by the redundant circuits, for example by Quadding or Tripling [4]. Triple Modular Redundancy (TMR), masking one fault [5, 6], uses three channels A, B, C and a Majority Voter [7,8]. A TMR Reliability Block Diagrams (RBD) is shown in Fig. 1.

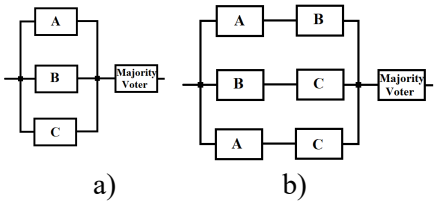


Figure 1 – TMR Reliability Block Diagrams: a) Conditional TMR Reliability Block Diagram; b) Real TMR Reliability Block Diagrams

Let P be the failure-free operation probability of a single channel, P_{MV} – the failure-free operation probability of the Majority Voter (MV). Then the failure-free operation probability of the TMR structure P_{TMR} according to the RBD shown in Fig. 1b) is described by the expression

$$P_{TMR} = (3 \cdot P^2 - 2 \cdot P^3) P_{MV}. \quad (1)$$

An Advanced TMR3 RBD masking one fault [5,6] in the channels and one fault in the Majority Voters, include three MV, is shown in Fig. 2:

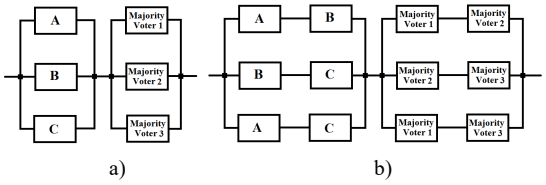
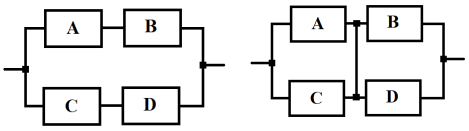


Figure 2 – Improved TMR3 RBD with three Majority Voter: a) Conditional TMR3 RBD; b) Real TMR3 RBD

Therefore, we get higher reliability according to the formula

$$P_{TMR3} = (3 \cdot P^2 - 2 \cdot P^3)(3 \cdot P_{MV}{}^2 - 2 \cdot P_{MV}{}^3). \quad (2)$$

The TMR circuit delay increases by the MV delay as compared to the original circuit. In addition, we need three power sources. Quadrupling, that is, using QR at the transistor level, masking one fault in the transistors A, B, C, D [5,6], does not require a voting device [9,10] (Fig. 3).



a) b)

Figure 3 – CMOS transistor Quad Structures: a) DNF option; b) CNF option-more connections A, B, C, D – corresponding MOS transistors

QR RBD is demonstrated in Fig. 4:

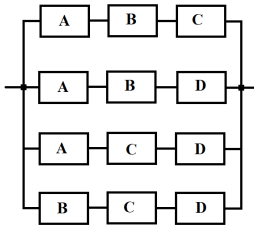


Figure 4 – QR Reliability Block Diagrams

Let P_{tr} be the failure-free operation probability of the single transistor, then the failure-free operation probability of the QR structure P_{QR}, according to the RBD shown in Fig. 4, is calculated by the formula

$$P_{QR} = P_{tr}{}^4 + 4 \cdot P_{tr}{}^3 (1 - P_{tr}). \quad (3)$$

Taking into account Weibull distribution [11], we get the failure-free operation probability of CMOS QR for *n* transistors:

$$P(t)_{QR} = [e^{-4 \cdot \lambda_{tr} \cdot t^{\alpha}} + 4 \cdot e^{-3 \cdot \lambda_{tr} \cdot t^{\alpha}} (1 - e^{-\lambda_{tr} \cdot t^{\alpha}})]^n, \quad (4)$$

where λ_{tr} – is the failure rate of one transistor (dimension 1/hour), t – is the operation time, $1 < \alpha < 2$ - is the Weibull distribution coefficient. The quadding circuit delay increases more than two times as compared to the original circuit. In the case of masking *r*-faults, we have the corresponding expressions for the Modular Redundancy (MR)

$$P_{MR:(r+1)\,from\,(2r+1)}(t) = \sum_{i=0}^{r} C_{2r+1}^{i+1} \{e^{-[(2r+1)-i] \cdot \lambda_{CH} \cdot t^{\alpha}} \cdot (1 - e^{-\lambda_{CH} \cdot t^{\alpha}})^i\} e^{-\lambda_{MV} \cdot t^{\alpha}}, \quad (5)$$

where λ_{CH} – is the failure rate of one channel, λ_{MV} - is the failure rate of the Majority Voter; or for the Quadratic Redundancy (QR):

$$P_{MR:(r+1)\,from\,(2r+1)}(t) = \sum_{i=0}^{r} C_{2r+1}^{i+1} \{e^{-[(2r+1)-i] \cdot \lambda_{CH} \cdot t^{\alpha}} \cdot (1 - e^{-\lambda_{CH} \cdot t^{\alpha}})^i\} e^{-\lambda_{MV} \cdot t^{\alpha}}, \quad (6)$$

Calculations show a higher efficiency of (6) as compared to (5). However, when applying (6) one runs into problems with observing the Mead-Conway constraints [12] and testing of the Quad CMOS circuits. At the same time, a TMP testing procedure is simply realized by, for example, switching off the power of one of the channels. The author proposes a method for verifying the Quad CMOS circuits based on controlling the power supply of the transistors substrates.

2. THE CMOS NOT SIMULATION

Let us consider the simplest CMOS gate, that is, the NOT gate, whose logical function is:

$$f(x) = \bar{x}. \quad (7)$$

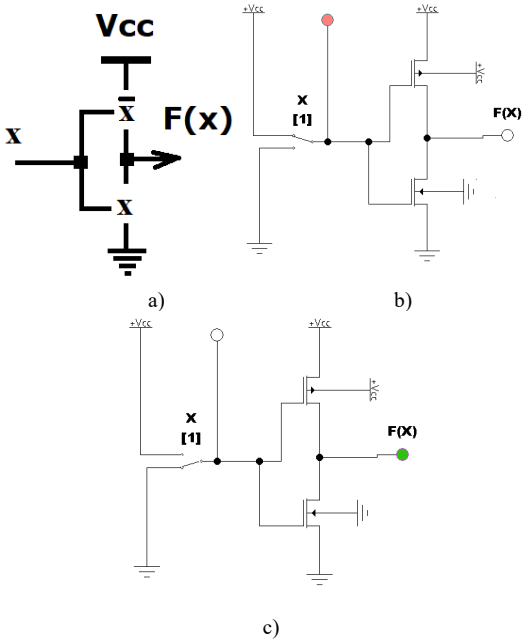
The power supply (+) switch function is described by the expression

$$f(x)_{+} = \bar{x}. \quad (8)$$

Ground (0) switch function is described by the inverse expression

$$f(x)_{0} = x. \quad (9)$$

The CMOS NOT Gate flowcharts are seen in Fig. 5.

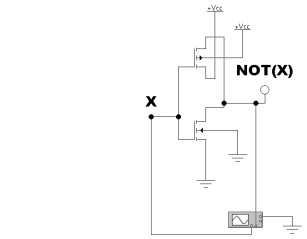


a) b)

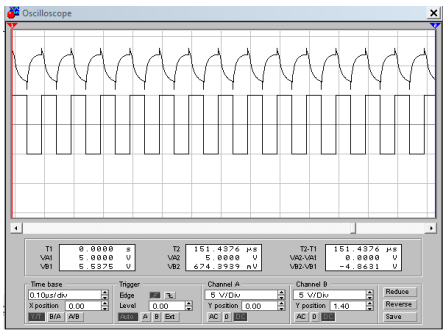
c)

Figure 5 – A CMOS NOT Gate: a) Conditional flowchart; b) Static simulation by the system NI Multisim x=0, F(x) =1; c) Simulation x=1, F(x) =0

In Fig. 5a), $\bar{x}$ means a *p*-MOS transistor, while x means an *n*-MOS transistor. A real MOS transistor has the Gate, Drain, Source, and Substrate, see, Figs. 5b) and 5c). The CMOS NOT Gate dynamic simulation by the system NI Multisim (National Instruments Electronics Workbench Group) is seen in Fig. 6.



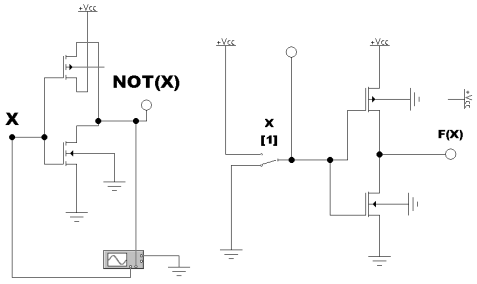
a)



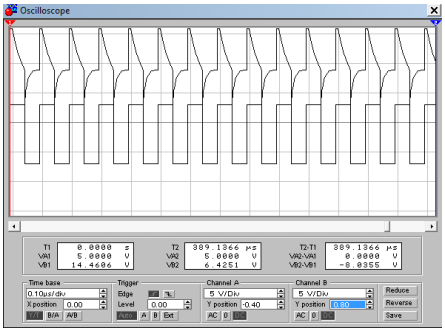
b)

Figure 6 – The CMOS NOT Gate dynamic simulation: a) CMOS NOT model; b) NOT normal waveform

In the case of disconnecting substrates, for example, of the *p*-MOS, we get a fault as shown in Fig. 7.



a)



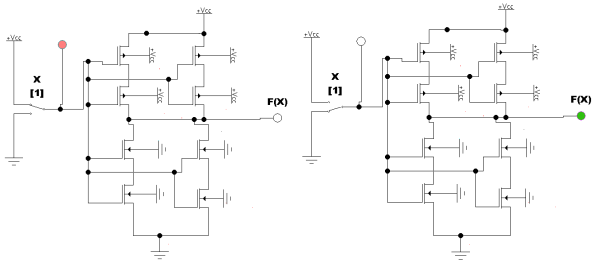
b)

Figure 7 – A Defect CMOS NOT Gate dynamic simulation: a) CMOS NOT model with disconnecting substrate of the p-MOS; b) NOT defect waveform

A similar picture is observed when the substrate of the second transistor *n*-MOS is disconnected.

3. THE QUAD CMOS NOT SIMULATION

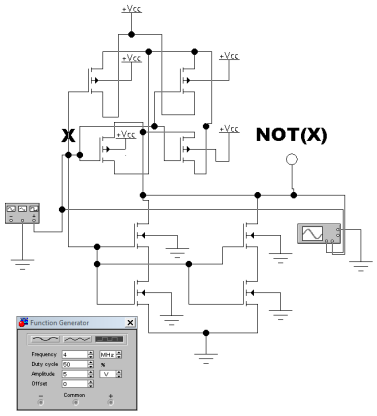
Including the quadding redundancy according to Fig. 3a) DNF option, we obtain a QR CMOS NOT model (Fig. 8).



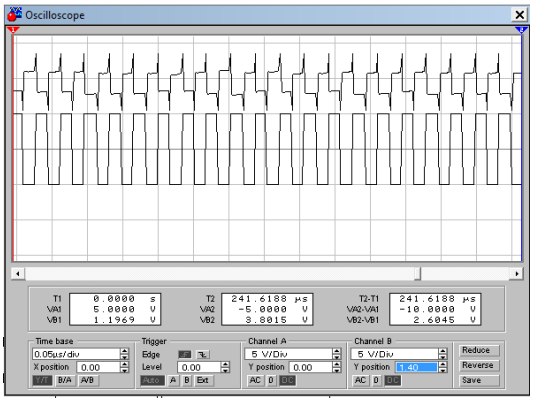
a) b)

Figure 8 – The Quad CMOS NOT Gate static simulation: a) x=1; F(x)=0; b) x=0; F(x)=1

The Quad CMOS NOT Gate dynamic simulation is illustrated in Fig. 9.



a)



b)

Figure 9 – The Quad CMOS NOT Gate dynamic simulation: a) Quad CMOS NOT model; b) Quad NOT normal waveform

With such a QR the delay is doubled since there are now not one but two transistors in each circuit. Nevertheless, it provides a fault tolerance - if one of

any transistors fails either in the upper or the lower parts of the circuit, or even in the upper and lower parts simultaneously:

$$AB \vee CD, (A = B = C = D) \Rightarrow AA \vee AA = A. \quad (10)$$

Turn off the substrate of one p-MOS, and we see that the model is workable, as presented in Fig. 10.

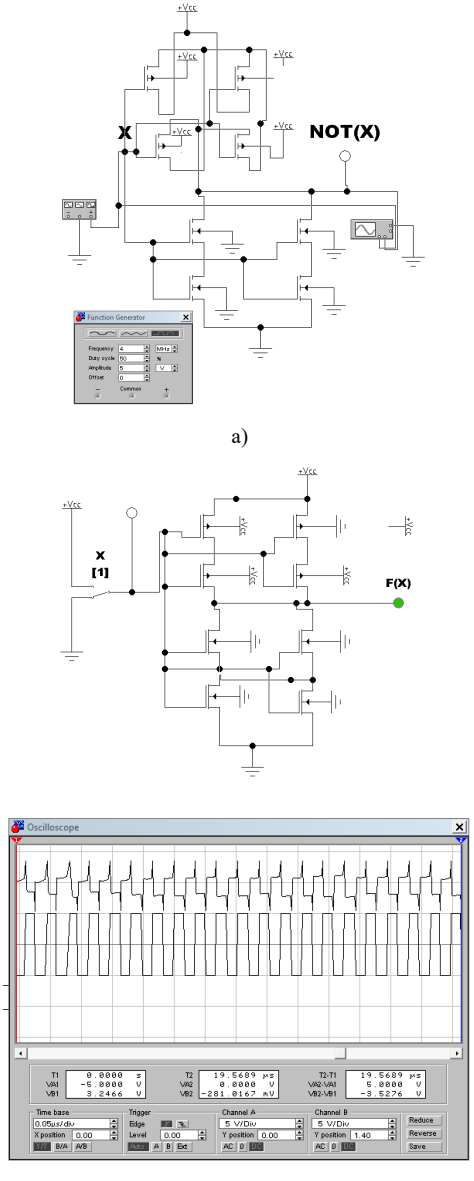


Figure 10 – A defect but workable Quad CMOS NOT Gate dynamic simulation: a) Quad CMOS NOT model with disconnecting substrate of one p-MOS; b) Quad NOT correct waveform

Similarly, we can verify that the circuit operates unchanged when the substrate of one transistor is turned off at the top and/or the bottom of the circuit, for example:

$$AA \vee A1 = A; AA \vee A0 = A;$$
$$AA \vee A\overline{A} = A; AA \vee AX = A. \quad (11)$$

However, if we disconnect two substrates at once in one part of the circuits, a failure occurs, the circuit goes into a fault state. A defect Quad CMOS NOT Gate simulation is represented in Fig. 11.

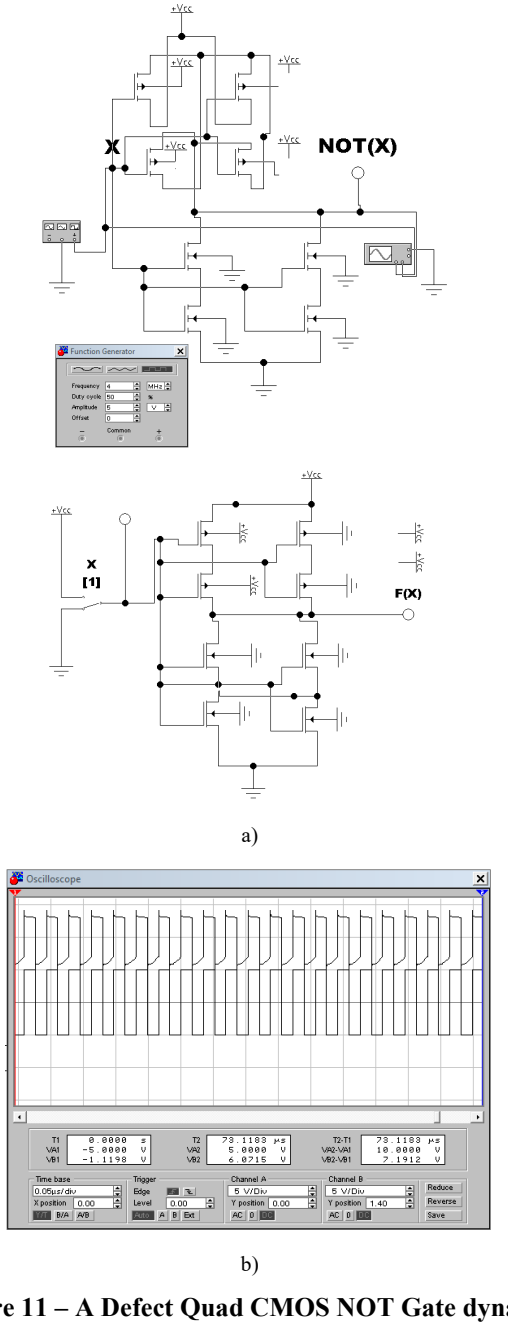


Figure 11 – A Defect Quad CMOS NOT Gate dynamic simulation: a) Quad CMOS NOT model with disconnecting substrate of two the p-MOS; b) Quad NOT defect waveform

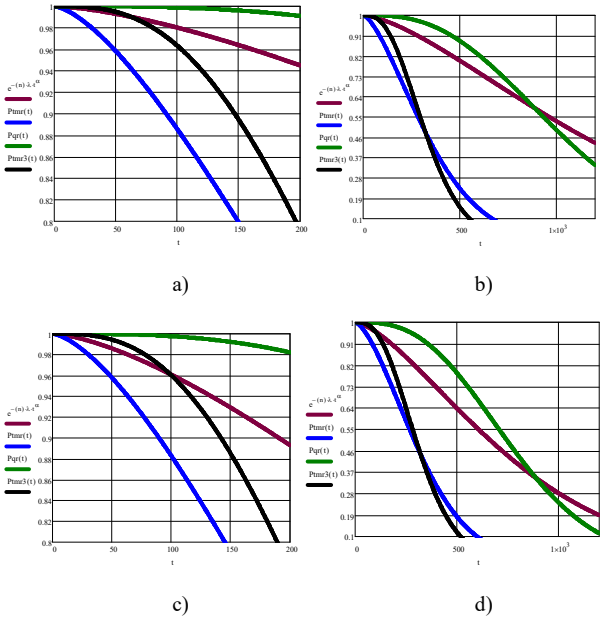
We see that in the case of disconnection of two or more substrates, the shape of the waveform changes, which explains the incorrect operation, for example:

$$AA \vee 11 = 1. \quad (12)$$

4. FAILURE FREE OPERATION PROBABILITY OF THE QR AND TMR, TMR3

Calculations with the PTC Mathcad [13] show (Fig. 12) that QR wins over a wide range of time, while TMR does not make sense, and TMR3 is

worse than QR and better than a non-redundant circuit on a small portion of the time axis, Fig. 12.



a) b)

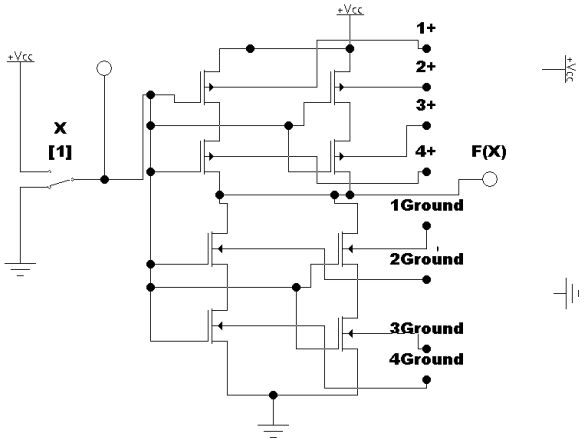
c) d)

Figure 12 – Failure-free operation probability curves of the n-transistors gate $e^{-n\cdot\lambda\cdot t^{\alpha}}$,gate with TMR $P_{tmr}(t)$,gate with TMR3 $P_{tmr3}(t)$,gate with QR $P_{gr}(t)$ ($\alpha=1,5;\lambda=10^{-5}$):a) n=2, t=0…200 hours; b)n=2, t=0…1000 hours; c) n=4, t=0…200 hours; d)n=4, t=0…1000 hours

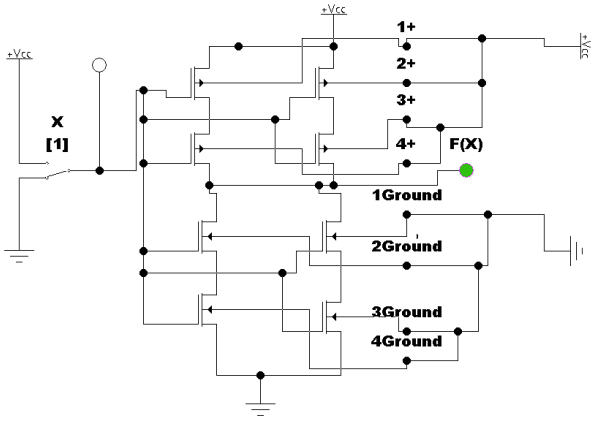
At the same time, the cost L in the number of the transistors QR is sometimes even smaller than in TMR. For example, let *n*=8 (2NOR-2AND or 2NANG-2OR gate), then L(TMR)=8*3+12 (Majority Voter)=36; L(TMR3)= 8*3+3*12 (Three Majority Voters)=60; L(QR)=4*8=32.

5. QR GATES AND PASS-TRANSISTORS CHECKING

The author proposes to introduce separate power supplies for transistor substrates: 1+;2+;3+;4+ for the p-MOS transistors and 1Ground; 2Ground; 3Ground; 4Ground for the n-MOS transistors (Fig. 13).



a)



b)

Figure 13 – Separate power supplies for transistor substrates: a) before checking state; b) after successful checking – ready to work

Tables 1 and 2 present the proposed QR Gate Checking procedure.

Table 1. QR up sub-circuit Gate Checking (n-MOS)

1+	2+	3+	4+	Result
+Vcc	+Vcc	+Vcc	+Vcc	Normal
+Vcc	+Vcc	+Vcc	Ground	Normal
+Vcc	+Vcc	Ground	+Vcc	Normal
+Vcc	+Vcc	Ground	Ground	~
+Vcc	Ground	+Vcc	+Vcc	Normal
+Vcc	Ground	+Vcc	Ground	~
+Vcc	Ground	Ground	+Vcc	~
+Vcc	Ground	Ground	Ground	Failure
Ground	+Vcc	+Vcc	+Vcc	Normal
Ground	+Vcc	+Vcc	Ground	~
Ground	+Vcc	Ground	+Vcc	~
Ground	+Vcc	Ground	Ground	Failure
Ground	Ground	+Vcc	+Vcc	~
Ground	Ground	+Vcc	Ground	Failure
Ground	Ground	Ground	+Vcc	Failure
Ground	Ground	Ground	Ground	Failure

Table 2. QR down sub-circuit Gate Checking (p-MOS).

Ground 1	Ground 2	Ground 3	Ground 4	Result
+Vcc	+Vcc	+Vcc	+Vcc	Failure
+Vcc	+Vcc	+Vcc	Ground	Failure
+Vcc	+Vcc	Ground	+Vcc	Failure
+Vcc	+Vcc	Ground	Ground	~
+Vcc	Ground	+Vcc	+Vcc	Failure

+Vcc	Ground	+Vcc	Ground	~
+Vcc	Ground	Ground	+Vcc	~
+Vcc	Ground	Ground	Ground	Normal
Ground	+Vcc	+Vcc	+Vcc	Failure
Ground	+Vcc	+Vcc	Ground	~
Ground	+Vcc	Ground	+Vcc	~
Ground	+Vcc	Ground	Ground	Normal
Ground	Ground	+Vcc	+Vcc	~
Ground	Ground	+Vcc	Ground	Normal
Ground	Ground	Ground	+Vcc	Normal
Ground	Ground	Ground	Ground	Normal

Analogically, for TMR [14-16], it is possible to introduce substrates power supply channels, for example for the LUT FPGA [17-20] p-MOS pass-transistors, as shown in Fig. 14.

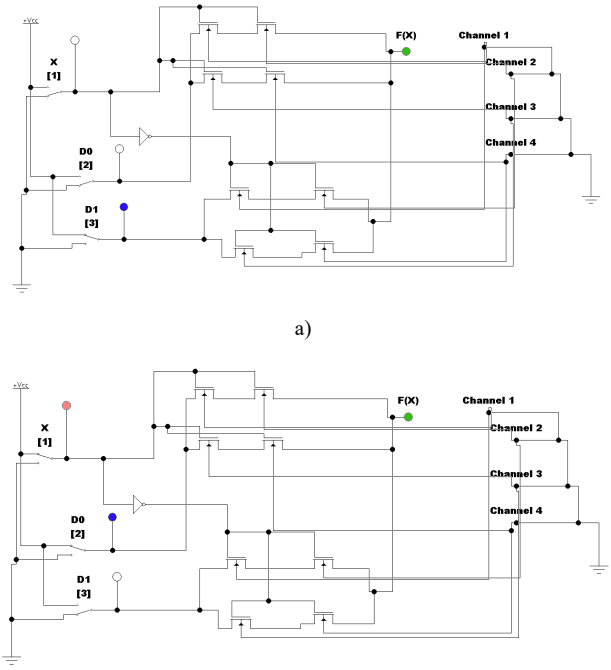


Figure 14 – Separate power supplies (Channel 1…Channel 4) for LUT-1 pass-transistor substrates: a) ready to work; x=0;D1=1; b) ready to work; x=1;D0=1

The invertor in Fig.14, in principle, must be a QR gate [21], like in Fig. 13.

6. CONCLUSIONS

Our results show that it is possible to check up the QR gates and pass-transistors circuits by the use of separate power inputs of the transistor's substrate. Testing with disconnection of substrates can be carried out first at the production stage and then connected to all relevant inputs of the power source and during the operation, for example, using relay switching. If the Mead-Conway restriction is satisfied, then the QR is (in some cases, paradoxically) even less costly than the TMR, since in the latter case, Majority Voters are needed. If a CMOS Majority Voter has 12 transistors, one output MOS QR n-transistor gate is "not more expensive" than CMOS TMR gate in case $n \le 12$. And if m is the number of CMOS circuit outputs, then in case $n \le 12m$. But the decomposition to comply with the Mead-Conway constraints worsens the efficiency of QR, so it is advisable to combine QR and TMR for the optimal design.

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Research interests include: methods and means of assessment and ensuring for reliability.